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COST EFFECTIVE, HIGH PERFORMANCE TRANSIENT RECORDER SYSTEMS, UTILIZING THE LATEST ADC'S, S/H'S, MEMORIES AND PLA'S

FINAL REPORT

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DISCLAIMER

ABSTRACT

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"COST EFFECTIVE, HIGH PERFORMANCE TRANSIENT RECORDER SYSTEMS UTILIZING THE LATEST ADC'S, S/H'S, MEMORIES AND PLA'S"

This project was to develop five transient recorder modules of various speeds and features. Four of the modules; TR200, 200MHZ recorder; TR2/25, Dual 25MHZ recorder; TR1012, 10MHZ, 12 bit recorder, and the ADC3216, 32 channel, 16 bit recorder were developed in the international CAMAC standard. The fifth unit, VTR1, 25MHZ recorder was packaged in the VME standard. Three of the modules, Models TR200, TR2/25 and VTR1 are already in Phase III. The ADC3216 has been prototyped and successfully evaluated by a number of customers. The last module, Model TR1012, has been completely designed and the artwork completed. This module will undergo tests shortly.

The modules have been well received and have accounted for over $250,000 in shipments over the last six months. Many of these shipments have been for evaluation and the quantities being discussed are impressive. We are satisfied with the effort we have expended and the help the government has provided to make all this possible. In addition to having improved specifications, the modules are also lower in cost. The government is our primary customer and they have already saved over $100,000 on the shipments we have made in this short time. Because of this we feel both our company and our country have benefited from this grant.

FINAL REPORT

In this final report we would first like to discuss the project in general and then each product separately. Customer satisfaction has been good regarding the products developed. They offer significant advantages over those previously available. They are smaller, consume less power, offer additional features and are lower in cost. Three of the modules have gone into Phase III already and we have made shipments totaling over $250,000. They have been well received by the users and we feel future sales should be substantial. In fact, if money was not so difficult to obtain at the present time, sales would have been much greater. The last two products will go into Phase III in the next few months and we feel from customers comments that they will also be well received.

We have used the grant to buy equipment which we could not afford ourselves and evaluate many new components. The modules that were designed offer features that were not available previously. The wide acceptance the new modules have received confirms to us the effort was worthwhile.

We must also admit we took on more than we bargained for in this endeavor. However, we have no regrets, we see there is a demand for the modules and this should help both our company and the country. We did ask for a nine month extension and feel we should explain the reasons. In actuality there was only one basic reason, the 200MHZ recorder. Our original intentions were that our fastest recorder would be 50 to 100MHZ. However, once we got into the project we saw a greater demand at 200MHZ and there were new parts that would make it

possible with significant advantages over current modules. We were able to develop the module and offer the following advantages:

1) *It was a double width module, while those previously available were five widths.*
2) *It used less than 30 watts of power, the others used over 110 watts.*
3) *The memory, either 64K or 256K, was mounted on board, which offers more reliable performance, especially at these speeds. The other recorders used external memory which was cabled to the recorder.*
4) *The clock frequency could be programmably controlled to provide sampling periods from 5nsec to 320nsec.*
5) *The module could also be operated in a burst mode so that importance sampling could be performed.*
6) *The memory was backed up with capacitors instead of batteries which have to be replaced to insure performance.*
7) *The module was designed with components that were capable of higher speeds than 200MHZ. This provided two advantages, the modules were simple to test and did not need to have voltages or timing trimmed. This offered a more reliable module and reduced testing time and expense.*
8) *The last feature which may prove the most important is cost. The module sells at 40% less than the competition. In addition it does not need the high powered expensive crates the current units require. You can put eleven of our modules in a standard crate and a maximum of four of the current ones in a special high powered crate. This means fewer crates, cabinets and space are necessary, an extra saving.*

The reason for the extension, however, was the difficulty we encountered with this module. While the design of the module was difficult, we were not prepared

for the problems of laying out the module. It contained both analog and digital circuits and operated at a clock frequency of 200MHZ. Because we wanted to offer the module and still make a profit, it was important that the final result be a reliable, trouble free design. With these requirements in mind we layed out the boards four times. We started with a two layer board and ended up using a four layer one. We were completely satisfied with the final results and are happy we went ahead with the 200MHZ design. It has been our best seller so far and the interest it is generating is very encouraging.

However, to develop this module took us two years, the total grant time and so the extension was required to complete the other four modules.

200MHZ, 8 BIT TRANSIENT RECORDER

MODEL TR200

In our report about the need for the nine month extension, we discussed the TR200 and feel this would be the one to begin with in this final report. Some of the things discussed regarding this module also pertain to the other modules and so will not be repeated in their sections.

First, let me say what we wanted from the grant was to design modules we could not afford to do on our own. We also wanted the modules to fit areas where there was a need for them. Our intent was to build good modules that there was a demand for and do it at a profit. We felt the government gave us this money so that we could make available products that were not presently available or were substantial improvements over present versions. We felt we had the moral obligation to spend the money wisely and come up with modules that would be valuable assets to the company. We feel this was accomplished and we are pleased with the results. In actual fact, to develop the modules cost us more than the grant allowed. So we are very pleased that the modules have created a lot of interest and can be sold at a profit. This means that the extra money spent by the company will be more than returned.

Our goal with all the modules was to develop reliable units that are easy to use and test. With the grant we were able to spend more time selecting components, had better equipment to lay out the boards and more sophisticated equipment for testing. These are all luxuries for a small business that must compete. We

feel we could have never accomplished what we did on our own. Although we are just beginning our Phase III effort, the savings to the government on our shipments so far are over $100,000.

An amplifier for the recorder was chosen that had a bandwidth of 200MHZ, and a high drive capability. Two of these were used to provide an overall bandwidth of 100MHZ. The first amplifier provided gain for the low level input. The second amplifier sums the low level input, the high level input and the programmable offset input. The second amplifier also provided the high drive capability we wanted for the ADC. The ADC we chose operated as a complete 8 bit flash converter at speeds of over 200mhz. We used a full 8 bit converter rather than a unit that does the conversion as a two step operation. This simplified the design and greatly improved the results. We were able to obtain an effective bit rate of over seven. The converter was ECL and its output was eight complimentary pairs. A lot of time was spent on this analog front end, primarily in an effort to reduce noise. With the module operating at 200MHZ, an analog amplifier perfectly able to pick up any stray noise caused quite a problem. This was one of the major layout problems and required four tries. The first on a double layer board and the next three on four layer boards. The final design actually incorporated each layer in a unique fashion and with this layout we were able to get good effective bit results.

There are only four adjustments used in the analog section. The ADC has two adjustments, one to set the full scale range and a mid scale adjustment for improved linearity. These are set with the low level input which has no adjustment. Then the high level amplifier is adjusted to match the low level input. An offset adjustment is provided for the second amplifier. The

programmed offset is generated using a DAC and amplifier. An adjustment is provided for the DAC output and the amplifier offset. These adjustments are very simple to make and can be done statically. There are no adjustments necessary for timing in the logic. The simplicity of this setup has a great bearing on the ease in which the module can be set. It means a more accurate, reliable unit and is one of the factors in our ability to significantly lower the price.

The differential output from the ADC is converted to single ended for storage using a differential, ECL receiver. Storing data at 5nsec is quite formidable. To obtain the density we wanted at these speeds we decided to break up the memory bank. The first level of storage is ECL latches. We break the output of the converter into two channels each operating at 100MHZ. A set of ECL latches is used to store the data for each internal channel. To get the density we required we then go to TTL levels, using ECL to TTL converters. We take the output of the ECL latches which have been converted to TTL and store them serially into two sets of eight 100MHZ 8 bit latches. After four of the latches are loaded, their data is loaded into four high speed memories with a capacity of 8K or 32K as an option. While this is happening the other four latches are being loaded for storage in the TTL memories. The storage capacity of the module is made up of eight high speed TTL chips, four for each internal channel. This memory can store 64K using 8KX8 memories or 256K when 32KX8 memories are used. By arranging the memory in this fashion we were able to achieve two important goals. We were able to provide the memory inside the module and avoid the problems of cabling the memory externally and lowering the power consumption dramatically..

The timing for the module was another critical feature. The internal timing is derived from an internal crystal oscillator and a high speed counter. This provided a programmable clock with a sampling rate of 5nsec to 320nsec. An external clock input was also provided and because of the clocking scheme, this could be varied. This allowed for such things as importance sampling. A slow clock could be used to monitor the signal and when an event occured the clock frequency could be increased.

The clocking will be described for 200MHZ operation. The output of the clock circuit is selected to be the 200MHZ signal. This signal is used to drive the ADC. It is also fed to a flip-flop whose output clocks each of the two 100MHZ data latches, one for each internal channel. This 100MHZ clock also drives two complimentary 100MHZ binary counters. These are divided and used to clock the eight high speed latches in each channel. After four latches are clocked a signal is sent to the large TTL memories to write data from those four latches while the next four are being loaded. Describing the timing is simple, performing it was quite complicated. Because the components chosen could easily perform at the speed required we did not have a problem with marginal waveshapes and timing. This greatly simplified the actual design. But the timing of all the various clocks was dependent on each other and so the final timing block had to produce the various pulses at the correct time. This was done by using high speed ECL gates as delays. As stated before,the signals used were very stable and had good waveshapes. The basic delays used were gates. The final result was a stable timing generator that required no trimming. The memory counters were high speed "F" type counters and were also triggered by this timing generator.

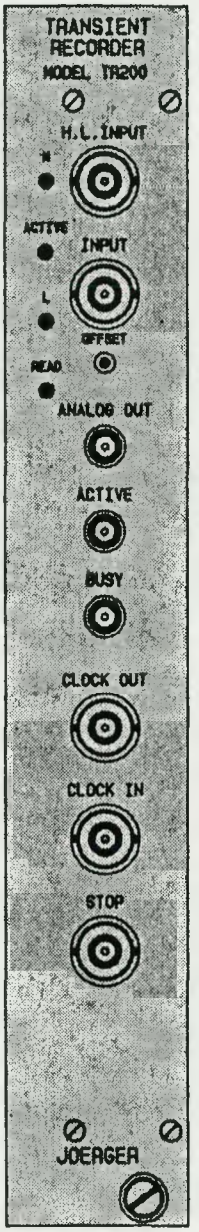
The CAMAC decoding was accomplished using a programmable logic device which saves a great deal of board space. The software was kept exactly like previous units. There were many systems already in use and the customers felt this would simplify their introduction. In reality they were correct, most of the initial units were used in existing setups.

There is a complete data sheet on the TR200 enclosed which fully describes its features.

Joerger ENTERPRISES, INC.

MODEL TR200

200MHZ TRANSIENT RECORDER



FEATURES:

- 200MHZ SAMPLING FREQUENCY
- 256K ON BOARD MEMORY, PROGRAMMABLE
- 8 BIT RESOLUTION
- DOUBLE WIDTH CAMAC MODULE
- LOW POWER CONSUMPTION, 27 WATTS
- PRE/POST-TRIGGER MODE
- INTERNAL OR VARIABLE EXTERNAL CLOCK (DC TO 200MHZ)
- HIGH SPEED DAC OUTPUT
- MEMORY BACKUP
- INPUT RANGE, UNIPOLAR OR BIPOLAR
- PROGRAMMABLE INPUT OFFSET ADJUSTMENT

The MODEL TR200 is a complete 200MHZ transient recorder packaged in a double width CAMAC module. It incorporates the latest developments in flash converters, high frequency amplifiers, fast dense memories and programmable logic. It contains an internal 256K memory so no other modules need be attached, simplifying its use and greatly improving its reliability. This module meets or exceeds the specifications of existing modules, is packaged in a double width module and uses less than 30 watts. This means that eleven of these converters can be packaged in a standard crate eliminating the problems of size and cooling that now exist.

This module is completely programmable so that it can be easily tailored to each application. The amount of active memory and the amount of pre- and post-triggering can be selected for efficient operation. Either an external clock or the internal crystal controlled clock can be chosen. The external clock can be from DC to 200MHZ and in addition can be varied during data acquisition to provide for bursting or importance sampling. With the internal clock, in addition to a 200MHZ clock, six other frequencies are available providing sampling times from 5nsec to 320nsec. To handle a wide range of input signals, a programmable offset adjustment is provided. This allows inputs from -512mv to +512mv to be accepted simply by programming the input offset.

The maximum memory size is 256K with 64K as standard. The active memory used for a particular run can be set so that recording time can be optimized. The active memory can be selected from 16K to 256K in 16K steps. The amount of pre-trigger recording can also be selected so that the pre/post-trigger ratio can be optimized. The active memory is divided into eighths and can be programmed to be all pre-trigger, all post-trigger or some ratio in between.

To monitor the data being converted during a run, a high speed digital to analog converter is provided. This takes the output of the data being latched from the ADC and generates an output signal that will track the input being supplied.

The programming for this module is completely compatible with units now in the field. This allows the incorporation of these units into existing systems with no need to change programming software.

SPECIFICATIONS

NORMAL INPUT LEVEL	512mv peak to peak.
INPUT IMPEDANCE	50 ohms ±2%
OFFSET	512mv, internally programmable with 8 bit resolution providing for both unipolar and bipolar inputs.
OVERLOAD PROTECTION	±7.5 volts D.C.
HIGH LEVEL INPUT	5.12v peak to peak.
INPUT IMPEDANCE	50 ohms ±2%
OFFSET	5.12 volts internally programmable with 8 bit resolution providing for both unipolar and bipolar inputs.
OVERLOAD PROTECTION	±7.5 volts D.C.
INPUT ANALOG BANDWIDTH	100MHZ
RESOLUTION	8 bits, straight binary.
CLOCK	
INTERNAL	200MHZ, crystal oscillator providing resolution of 5, 10, 20, 40, 80, 160, 320nsec. Stability ±.01%
EXTERNAL	0 to 200MHZ may be varied or operated in a burst mode.ECL input levels standard, NIM levels optional.
CLOCK OUTPUT	An output clock is provided that is the same frequency that the module has been programmed to operate. It is available continuously in either the internal or external clock mode. This may be used for timing or driving additional recorders. The standard output is ECL. NIM levels available as an option.

MEMORY	256K maximum, 64K standard. Programmably selected in 16K steps from16K to 256K.
PRE-TRIGGER SAMPLE SIZE	Programmably selected from 0/8 of active memory "Post-trigger Mode" to 8/8 of active memory "Pre-trigger Mode".

FRONT PANEL SIGNALS

ANALOG OUTPUT	A DAC output is provided to monitor the converted input data during data acquisition. 1 volt into a 50 ohm load.
ACTIVE OUTPUT	A TTL signal is generated to indicate the recorder is active.
STOP INPUT	A stop trigger initiates the post-trigger mode. It is jumper selectable to accept either a positive or negative signal and is terminated in 50 ohms. To facilitate various signals the input threshold can be varied from +1 volt to -1 volt.
BUSY OUTPUT	A TTL signal is generated to indicate that the recorder has received a stop trigger and is in the post-trigger mode.
OFFSET TEST POINT	Provides the ability to monitor the programmed input offset.

INDICATORS

N	Module has been addressed on its N line.
ACTIVE	The module is acquiring data.
L	The module has completed its data acquisition cycle.
READ	The module is in the readout mode.

CAMAC COMMANDS

0o	Reads module status register, pre-trigger size, internal or external clock, clock frequency, active memory size.
1o	Reads offset register.
2o	Data readout, two data bytes read out for each command, 16 bits, low order address on R1-8 and next higher address on R9-16. When memory is completely read out a Q=0 is returned. Q=1 is returned if a data cycle has been completed and an F17 command has been performed. Memory readout begins at the first word recorded and continues to the last word recorded. No interigation is required.
3o	Reads module identifier.
8o	Tests LAM, Q=1 if set and enabled.
9o	Activates module, clears LAM and starts digitizing mode.
10o	Clears LAM.

16o — Writes the modules status, selects the active memory, pre-trigger size, internal or external clock and the internal clock frequency.

R1-4 Pre-Trigger	R5-R7 Sample Period	R9-R12 Active Memory Size
0 0/8 of Active Memory	0 5nsec.	0 16K
1 1/8 of Active Memory	1 10nsec.	1 32K
2 2/8 of Active Memory	2 20nsec.	2 48K
3 3/8 of Active Memory	3 40nsec.	3 64K
4 4/8 of Active Memory	4 80nsec.	4 80K
5 5/8 of Active Memory	5 160nsec.	'
6 6/8 of Active Memory	6 320nsec.	'
7 7/8 of Active Memory	7 Ext. Clock	15 256K
8 8/8 of Active Memory		

17o — Enables data readout, sets address counter to first active channel, F2 is used for readout.

19o — Writes offset register.

24o — Disables LAM.

25o — Stop command, the module will perform the required number of post-trigger samples, stop the cycle and set the LAM flip-flop.

26o — Enables LAM.

27o — Tests LAM, Q=1 if LAM set.

X — An X response is generated for all valid commands.

Q — A Q response is generated for F0, 1, 3, 9, 16, 17, 19 and when appropriate for F2, 8, 27. If the module is active only F25 generates a Q.

L — An L response is generated if the cycle has been completed and the modules L response is enabled.

Z•S2 — Resets module.

POWER REQUIREMENTS +6v, 2.4A Total 27 watts.
-6v, 2.1A
Memory backup on board.

SIZE Double width CAMAC module.

TEMPERATURE RANGE 20° to 50°C

OPTIONS TR200-256 TR200 with an internal memory of 256K

JEI0489

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DUAL CHANNEL 25MHZ TRANSIENT RECORDER

MODEL TR2/25

There are a number of 25MHZ, single channel recorders on the market with 8K of memory. Their designs were fairly old and we felt with the components now available much more could be offered. The result of our efforts yielded the Model TR2/25. This has two 25MHZ recorders and up to 64K of memory per channel in a single width CAMAC module. In addition to this, it has all the other features of existing 25MHZ recorders. What it offers the customer is two 25MHZ recorders in a single width CAMAC module at a cost savings of up to 25%. This does not take into consideration that twice the number can be put in a crate for an additional savings in crates. It also offers the user the ability to increase the memory size of each channel from the 8K standard to 64K.

The input amplifier sums the input signal with a front panel controlled offset. This provides the ability for the module to accept a wide variety of input signals. The amplifier drives an eight bit high speed flash ADC. To suppress noise in the analog front end, separate isolated grounds are usedfor each channel. In addition, each power line to the front end of each channel is separately filtered. This helped significantly in reducing the noise and increasing the effective bit level. The output of the ADC is TTL and is fed to high speed latches where it is clocked at the completion of a conversion. The output of this latch is used to drive the data input of the memory. The standard memory is 8KX8 but as an option it can be supplied with either 32K or 64K per channel. When the module is not active the data in either of the memory banks can be monitored visually. Either channel 0 or 1 can be programmed to

read out. The selected channel's memory and address counter are activated and scanned. The data out of the memory is sent to an eight bit DAC whose output is buffered and brought to the front panel. A sync signal is also supplied so that the data recorded can be displayed on a scope for evaluation.

The internal clock is programmable and is derived from a 25MHZ crystal oscillator. It provides sampling speeds of 40nsec to 2560usec. An external clock input is also provided and can be any frequency from 0 to 25MHZ. It is also possible to importance sample with the external clock. The memory size can be programmed in 1K steps and the pre/post-trigger cycle can be set from all post-trigger to 7/8 pre-trigger 1/8 post-trigger. These programmable features allow the module to be set up for a wide variety of applications. The dataway logic is decoded in a programmable logic array which simplifies the module and saves board space.

A complete data sheet on this unit is provided which discusses its features and the CAMAC commands used.

This module has also proceeded to Phase III and a number have been shipped. One laboratory has bought a number just for evaluation. They have a very large requirement for them and if it satisfies their requirements they have told us that these modules are preferred. They feel the density, price savings and additional features makes them stand out over the others available. We should know shortly how it performed for them and if indeed they will purchase more.

Joerger ENTERPRISES, INC.

MODEL TR2/25

DUAL CHANNEL, 25MHZ, TRANSIENT RECORDER

FEATURES:

- DUAL CHANNEL TRANSIENT RECORDER
- 64K STATIC MEMORY PER CHANNEL
- 8 BIT RESOLUTION
- 25MHZ CLOCK RATE
- PROGRAMMABLE INTERNAL CRYSTAL CONTROLLED CLOCK
- EXTERNAL CLOCK INPUT, VARIABLE
- MEMORY SIZE PROGRAMMABLE IN 1K INCREMENTS
- PRE-TRIGGER RECORDING
- PRE/POST-TRIGGER RATIO PROGRAMMABLE
- SCOPE DISPLAY OUTPUT
- SINGLE WIDTH CAMAC MODULE
- POWER BACKUP FOR DATA RETENTION
- FRONT PANEL DISPLAY OF STATUS

The MODEL TR2/25, utilizing the latest advances in memories, amplifiers, flash ADC's and programmable arrays, makes possible the packaging of two complete 25MHZ transient recorders in a single width CAMAC module. To make the module even more attractive, each channel offers 64K of memory, eight times that available at present. To simplify its use it is completely programmable. The active memory size, the ratio of post and pre-triggering, the clock source and the frequency can all be programmably selected. Its status can be verified either by reading it on the dataway or visually on a front panel display. These features are made available so that the module can be taylored to the application it is to perform. The memory size can be selected from 1K to 64K in 1K steps. The ratio of pre-trigger and post-trigger data can be selected from 0/8" Post Trigger Mode" to 7/8 of the memory selected. The internal clock can be selected to provide conversion times of 40 nanoseconds to 2.56 microseconds. An external clock can also be chosen with an input range of D.C. to 25MHZ. This clock can be varied during an acquisition cycle so that importance sampling and bursting can be performed.

Operation of the module is quite simple. First, the module is programmed for the amount of active memory required for the application, the amount of pre-triggering needed, whether an external or internal clock will be used and if the internal clock is chosen, the clock frequency desired.

The module is then activated either manually via the front panel switch or by a dataway command. This triggers both channels into the record mode and digitizing begins. This will continue until the module receives a Stop signal from either a front panel signal or a dataway command. When this signal is received digitizing continues until the number of programmed post-trigger measurements have been performed. At this time the address of the last word recorded is stored and an interrupt is generated that indicates the cycle is complete.

The module can be read out either digitally via the dataway or visually using its digital to analog converter. Either channel can be commanded to read out. A sync signal is supplied for the display. The data in memory is kept until another cycle is performed so that data may be reread. Each data readout cycle is enabled with command F17 which loads the first address into the address counter.

SPECIFICATIONS (EACH CHANNEL)

ANALOG INPUT	512mv standard, 5.12v optional.
OFFSET	Front panel adjust, with test point, full scale adjustment
INPUT IMPEDANCE	50 ohms ±2% standard, 1K ohms optional.
BANDWIDTH	25MHZ minimum.
CONVERSION RATE	Internal, 25MHZ crystal controlled oscillator, sample time programmable from 40nsec to 2.56 micro sec. External clock, D.C. to 25MHZ, variable.
RESOLUTION	8 bits.
MEMORY	8K standard, 64K optional, programmable in 1K steps.
PRE-TRIGGER SAMPLES	The ratio of pre-trigger to post-trigger samples can be selected from 0/8 to 7/8 of programmed memory size. 0/8 is equivalent to post-trigger mode.
CLOCK INPUT	TTL pulse.
CLOCK OUTPUT	TTL output of clock being used in the module.
STOP INPUT	TTL pulse, negative going, will trigger the STOP MODE and after the programmed number of measurements is completed the cycle will stop and trigger a LAM.
ANALOG OUTPUT	A digital to analog converter is provided and Channel 0 or Channel 1 can be programmably selected for display when the module is not active.
DISPLAY SYNC	A TTL pulse is provided for triggering a scope.
MANUAL CONTROL	A front panel START-STOP switch is provided to manually control a cycle.

CAMAC COMMANDS

0o Reads out the modules status which includes the programmably selected active memory, pre-trigger samples and the sampling frequency being used (same for both channels).

2o Reads out the data recorded in Channel 0 on R1-8. When the last active channel is read out a Q=0 response is generated. This signal must be preceded by an F17 command which loads the first address.

2ı Same as 2o except reads out data from Channel 1.

3o Reads module identity and the amount of memory contained.

8o Tests LAM, Q=1 if LAM is set and enabled.

9o Activates a data acquisition cycle, clears LAM.

10o Clears LAM.

16o Sets modules status

R1-R4 Pretrigger	R5-R7 Sample Period	R9-R14 Active Memory
0 0/8 Active Mem.	0 40nsec.	0 1K
1 1/8 " "	1 80nsec.	1 2K
2 2/8 " "	2 160nsec.	2 3K
3 3/8 " "	3 320nsec.	3 4K
4 4/8 " "	4 640nsec.	'
5 5/8 " "	5 1280nsec.	'
6 6/8 " "	6 2560nsec.	'
7 7/8 " "	7 Ext. Clk.	63 64K

17o Enables readout mode, loads first address.

18o Enables Channel 0 display if module not active.

18ı Enables Channel 1 display if module not active.

24o Disables LAM.

25o Stop cycle trigger.

26o Enables LAM.

27o Tests LAM.

X All commands generate an X response.

Q F0 and F3 generate a Q response, if module is not active (taking data)commands F2, F16 F17 and F18 are operable and generate a Q response. A Q=1 is generated in response to F8 if LAM is set and enabled, and F27 if LAM is set.

L An L response is generated if the cycle has been completed and the modules L response is enabled.

(Z+C)S2 Clears module.

POWER REQUIREMENTS	±6V. Battery backup for data memory and status registers is available as an option.	
SIZE	Single width CAMAC module.	
TEMPERATURE RANGE	20° to 50°C	
OPTIONS	TR2/25-16	TR2/25 with 16K of memory
	TR2/25-32	TR2/25 with 32K of memory
	TR2/25-64	TR2/25 with 64K of memory

JEI0489

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25MHZ VME TRANSIENT RECORDER

MODEL VTR1

The VME bus is becoming very popular and it has no transient recorders available. We felt this would be a good product to introduce. We already had a design for a 25MHZ recorder and felt this would be a good one to impliment on a VME board. In discussing this with a number of potential users we found two customers who had applications for a recorder in their VME systems. Their requirements were basically similar, the only difference being their input levels, which was easy to handle. They had a large memory requirement and so the memory was set at 64K. Using the same basic front end used in the Model TR2/25 we laid out the module.

This was our first VME module and the grant allowed us to look into this application. Before we got very far into it we already had two customers. Everything looked fine, we had the money, the circuitry and the customers. We gained a lot of experience with VME and delivered about a dozen modules. We also learned some other things about VME that were very enlightening. We want this report to be an honest account of our experiences and so we must say we were not too happy with the VME system. It does offer a higher speed bus and a well thought out pin arrangement for the dataway. The problem we felt was that the board was physically to small for a functional module. For microprocessors, memory and other devices which offer the use of high density chips they are probably fine. But for a functional module that must interface to the outside

world and perform some function, the room on the board was not sufficient in our case. The bus interfacing is reasonably complex and takes up a lot of board area. I am aware there are chips being designed now to perform this interface but a year ago the one we found was very expensive, especially to use on a slave module. I am sure this either has changed or will change, but to what extent I do not know. As I said, we learned alot from this VME experience. We liked the bus but not the board. Since then we have come across the VXI bus. This is basically the VME bus with extras. The top connector is the same and the middle connector keeps the same pin assignments as VME. However, in VME there were a number of pins not assigned, in VXI these have been assigned. VXI also added a third connector which is set up for high speed operation. But the obvious advantage VXI would offer us is the board size. The VXI board is twice as deep and so provides much more available space. There is a strong possibility that we may take the experience gained with the VME recorder and do it again in VXI. We feel we could put all the features of our dual channel 25MHZ recorder on a VXI board and give the customer a more valuable product. The VME recorder was only a single channel, with all the programming done with on-board switches which could not be read out for verification.

Although we did not look into VXI extensively, a few facts did catch our attention. The modules are wider and a number of shielding options are presented as standard features. Although VME modules could be shielded, and in fact ours was, VXI seems to have looked into this more thoroughly. Also noticed was that the third connector, the high speed one, had as a feature a 100MHZ clock source. Somehow a 100MHZ recorder seems very appealing, possibly a product for the future.

In any case the VME experience we feel was useful for us. We have a product and customers who have an application for it. It also enlightened us about VME and brought our attention to VXI.

A complete data sheet on our VME recorder, Model VTR1, is included which describes its features and its VME interface.

Joerger ENTERPRISES, INC.

MODEL VTR1

25MHZ TRANSIENT RECORDER, PACKAGED IN VME

FEATURES:

- VME COMPATIBLE
- 25MHZ TRANSIENT RECORDER
- INTERNAL 64K MEMORY
- 8 BIT RESOLUTION
- INTERNAL OR EXTERNAL CLOCK
- PROGRAMMABLE CRYSTAL CONTROLLED OSCILLATOR

The Joerger Enterprises, Inc. MODEL VTR1 is a high speed transient recorder packaged in a double height VME module. The latest advances in flash ADC's, amplifiers and high speed memories are utilized to make this a completely self-contained recorder. It accepts an analog input, digitizes it with an internally programmable crystal controlled clock or an external clock and loads the data into an on board 64K memory. Data is read out in a two byte format, 16 bits at a time.

This module is programmed by internal switches. Two eight position switches are provided to select addresses, one for Data Readout and one for Status Read and Command Write. A switch for Interrupt Select and one for Interrupt Vector are provided. To select the clock the module uses one four position switch which selects Internal or External clock and the frequency of the internal clock.

A cycle is activated with an ARM signal. This resets the module and activates the front end. A START signal or GATE signal starts the cycle and the module begins digitizing the input signal. Data is loaded synchronously with the clock. In response to a STOP signal or the removal of the GATE signal, the cycle stops. At this point the last address is stored and an Interrupt flip-flop and a Cycle Complete flip-flop are set.

The output of the Interrupt flip-flop will generate an Interrupt Request signal on one of the seven lines selected. The Interrrupt and Cycle Complete signals also go to the status register so they can be monitored by the system. The Interrupt flip-flop is reset after an Interrupt Acknowledge cycle has been performed and the Cycle Complete signal is reset when the module is cleared.

A cycle may also be performed using the system Write commands, ARM, START and STOP.

SPECIFICATIONS

ANALOG INPUT	±10 volts, 1K ohms input impedance.
	512mv, 50 ohms optional.
OFFSET	A front panel offset and test point is provided.
RESOLUTION	8 bits.
INTERNAL CLOCK TIMING	25MHZ crystal controlled clock providing sampling rates of 40nsec, 80ns, 160ns, 320ns, 640ns, 1.28us, 2.56us or 5.12usec, switch selectable.
EXTERNAL CLOCK	DC to 25MHZ, may be varied during cycle to provide bursting or importance sampling.

EXTERNAL INPUT SIGNALS START, STOP, GATE, ARM	+2.5 volts, 50 ohms input impedance, 1K ohm optional.
INTERNAL SWITCHES	
STANDARD ADDRESS	Eight position switch to select data readout address, A16-A23.
SHORT ADDRESS	Eight position switch to select the address used to read module status and write commands, A08-A15.
INTERRUPT VECTOR	An eight position switch is provided to generate the interrupt status word that will be activated in response to an Interrupt Acknowledge.
INTERRUPT SELECT	A seven position switch is provided to select any one of seven Interrupt Request lines when an interrupt signal is generated indicating cycle is complete.
INTERNAL OR EXTERNAL CLOCK	A switch is provided to select either the programmable internal crystal oscillator or the external clock.
INTERNAL CLOCK FREQUENCY	A three position switch is provided to select the clock frequency to be used by the module.

COMMANDS

READ DATA	Standard address, AM=39 or 3D, module address on lines A16-A23, WRITE, LWORD and IACK high, module not taking data and strobes DSO, DS1. If these conditions are met themodule responds with DTACK and presents two 8 bit data words on data lines D00 to D15, for the address on A01 to A15.
READ STATUS	Short address, AM=29 or 2D, module address on lines A08 to A15, WRITE, LWORD and IACK high and strobes DS0, DS1. Read out is on data lines D00 to D07. The status word contains the condition of the module, ACTIVE, CYCLE COMPLETE, INTERRUPT, INTERNAL OR EXTERNAL CLOCK, PROGRAMMED FREQUENCY, MEMORY FULL.
WRITE COMMAND	Short address, AM=29 or 2D, module address on lines A08 to A15 WRITE low and LWORD and IACK high and strobes DSO, DS1. If these conditions are met the module can be commanded to ARM, START or STOP with data on data lines D00, D01, D02.
SYSRESET	In response to this signal the module resets and arms itself in preparation to perform a data acquisition cycle.

POWER REQUIREMENTS +5v, 1400ma
+12v, 80ma
- 12v, 140ma

JE10589

Joerger ENTERPRISES, INC.

166 LAUREL ROAD • EAST NORTHPORT, NY 11731, U.S.A. • (516) 757-6200

32 CHANNEL, 16 BIT SCANNING TRANSIENT RECORDER AND ADC

MODEL ADC3216

This module was designed in response to a large number of inquiries into higher resolution ADC's. It is meant to be used as either a scanning ADC or transient recorder. It is capable of handling up to 32 input channels and converting the analog input to digital with a resolution of 16 bits. It has a conversion time of 50usec and while not as fast as the other modules we designed in this grant, it is a very respectable speed for a 16 bit conversion. The module is completely programmable. It can be set to operate as a scanning ADC or transient recorder. The number of active channels can be selected, the clock rate and the amount of active memory are also programmable. It was designed to operate in many modes and provide 16 bit resolution.

The 32 differential inputs are sent to a 32 channel multiplexer. The output of the multiplexer is then sent to a differential amplifier. There are two amplifiers to choose from. The standard amplifier offers an input impedance of 50K ohm and a 50usec cycle time. The second uses an instrumentation amplifier offering 100M ohm input impedance and a scan time of 100usec per channel. The output of the selected amplifier then goes to an optional sample and hold input. This has an aperture jitter of 150psec. Once the amplifier is switched to the hold mode, the ADC will convert this level ignoring any variations that may be on the actual input signal. The output is supplied to a high speed 16 bit ADC for conversion. The input range of the ADC may be changed by the use of jumpers for either bipolar or unipolar operation. The output of the ADC is fed to a 16 bit latch which stores this data while it is being loaded into the memory. The standard memory is 16X8K and as an option, 16X32K and 16X64K are offered.

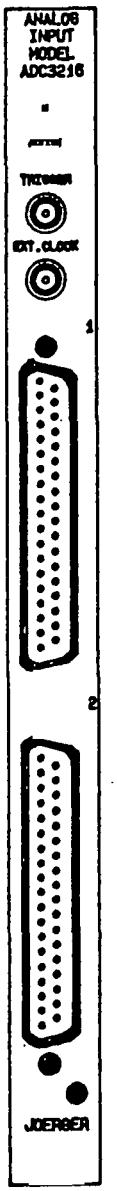
The module is completely programmable. The operating modes; Scanning ADC, Transient Recorder and operating the transient recorder in a burst mode, are selected from the dataway. The active memory size, the number of channels active and the clock frequency in the recorder mode are also programmable. The module can also reread this data to confirm the status of the unit. To eliminate problems with addressing, all the counters are high speed "F" types. The decoding is done with a programmable logic chip which both simplifies the design and saves a considerable amount of board space.

The prototype has been evaluated by a number of customers and they were very satisfied with the results. It has also been taken to a number of trade shows. The artwork has been corrected and is ready for production. The Phase III effort has already started on this module. A complete data sheet is included in this report which contains its specifications and command structure.

Joerger ENTERPRISES, INC.

MODEL ADC3216

32 CHANNEL, 16 BIT ADC



FEATURES:

- *16 BIT RESOLUTION*
- *32 CHANNELS, PROGRAMMABLE*
- *THREE MODES: SCANNING ADC*
  TRANSIENT RECORDER
  BURST MODE RECORDING
- *64K MEMORY, PROGRAMMABLE*
- *CRYSTAL CONTROLLED CLOCK*
- *INSTRUMENT AMPLIFIER INPUT*
- *SINGLE WIDTH CAMAC MODULE*
- *SAMPLE AND HOLD*

The Model ADC3216 can accept up to 32 differential inputs and digitize each with a resolution of 16 bits. The converted results are stored in on board memory for readout over the dataway. F0 or F1 and the appropriate subaddress provide the ability to read out individual channels, with internal logic to insure no conflict with data update. A scan mode readout is provided using F2. To improve the modules usefulness, it can be operated in any of three modes. As a scanning ADC, a transient recorder or in a burst mode. Inburst mode the module, in response to a trigger input, will scan the active channels once and stop. It will do this for each trigger until the active memory has been filled. At that time it will stop the cycle and generate a LAM.

The module is completely programmable. It provides the ability to set the operating mode, the number of active channels, and the active memory size. In the transient recorder mode the scanning speed is controlled by either an internal crystal or an external clock. The maximum scanning speed is determined by the choice of input amplifiers. The standard input is 50K ohms providing a scanning speed of 50usec per channel. As an option an instrument amplifier is available with an input impedance of 100M ohms and a scan rate of 100usec per channel. A sample and hold feature is also available as an option which greatly improves the actual acquisition time and in so doing provides improved performance. This module has been designed for versatility and ease of use while still providing the high accuracy 16 bits requires. High speed multiplexers, dense memories and programmable logic have been incorporated to provide all these features in a single width CAMAC module.

SPECIFICATIONS

ANALOG INPUT	*±5, ±10, +5, +10 volts differential.*
ACCURACY	*±.003% of FSR.*
INPUT IMPEDANCE	*50K ohms, 100M ohms optional.*

SAMPLE AND HOLD OPTION	
Accuracy	*16 bits*
Aperture Jitter	*150psec.*
SCANNING SPEED	*50usec. per channel, 100usec. with the high impedance instrumentation amplifier.*
CHANNELS	*32 differential inputs, programmably selected.*
MEMORY	*8K standard. 32K, 64K optional.*
EXTERNAL CLOCK INPUT	*TTL level.*
TRIGGER INPUT	*TTL level.*

CAMAC COMMANDS

0x	*Reads out data from Channels 0-15 in ADC mode.*
1x	*Reads out data from Channels 16-31 in ADC mode.*
2o	*Reads out data in scan mode when module is set to operate as a transient recorder. Q=0 is returned after last word is read out.*
3o	*Reads module identity, options and memory capacity.*
4o	*Reads module status.*
6o	*Reads active memory size the module is programmed to use.*
8o	*Tests LAM, Q=1 if LAM is set and enabled.*
9o	*Resets module.*
10o	*Clears LAM.*
16o	*Writes module status. Selects ADC, transient recorder, or burst mode. Selects number of active channels and selects internal or external clock and the internal clock frequency when in the transient recorder mode.*
17o	*Sets active memory size.*
24o	*Disables LAM.*
25o	*Start command.*
26o	*Enables LAM.*
27o	*Tests LAM.*
X	*An X response is generated for all valid commands.*
Q	*A Q response is generated for F0, 1, 3, 4, 6, 16, 17, and when appropriate for F2, 8, 27.*
L	*An L response is generated in the transient recorder mode if the cycle has been completed and the response is enabled.*
(Z+C)S2	*Resets module.*

POWER REQUIREMENTS: *±6, ±24 volts.*

SIZE: *Single width CAMAC module.*

TEMPERATURE RANGE: *20° to 50°C.*

OPTIONS:

ADC3216-32 32K MEMORY
ADC3216-64 64K MEMORY
INSTRUMENT INPUT AMPLIFIER
SAMPLE AND HOLD

JEI1089

Joerger ENTERPRISES, INC.
166 LAUREL ROAD · EAST NORTHPORT, NY 11731, U.S.A. · (516) 757-6200

10MHZ, 12 BIT TRANSIENT RECORDER

MODEL TR1012

There is a requirement for a fast, higher resolution recorder. The Model TR1012 is our response to this requirement. It has a resolution of 12 bits and can operate at a speed of 10MHZ. It has all the features of our other recorders. It can operate in a pre/post-trigger mode. The active memory size can be selected. An external clock can be used or an internal crystal clock can be used which has a programmable range of 100nsec to 20usec. Please note, the data sheet enclosed was an early version and contains an error. In the layout we wanted to keep the board a single width CAMAC module and we were not able to provide the 256K memory. The memory is 64K.

The standard input is ±1.25v into 1.5Mohms, with 50 ohms as an option. Another input is also offered as an option. It has a ±1.25v input into 1K ohm but has a front panel offset adjustment. The output from the amplifier goes to a 10MHZ, 12 bit ADC. To insure a good environment for the ADC it has a heavy ground plane, the ±15 volts it uses comes from a tracking regulator and the ±5 volts both for the analog and digital circuitry is heavily filtered. The output of the ADC is latched and the outputs of the latches are used to drive the 64K high speed memories. The address counters for the memories are high speed "F" type to insure accurate timing.

The modules operation is completely programmable. The pre/post-trigger ratio can be set, the clock can be either externally supplied or a programmable internal crystal controlled clock which can be set from 100nsec to 20usec. The

size of the active memory can also be selected from 512 to 64K words. The modules status can also be read out providing the ability to confirm its setup. When the module is not active, the data stored in memory can be visually displayed. A command is provided that scans the memory and sends the data to a 12 bit DAC. The output of the DAC, along with a sync signal, is supplied at the front panel for viewing on a scope.

The dataway logic is decoded in a programmable logic array which simplifies the task and saves a great deal of room on the board. A data sheet is supplied that lists the module's specifications and the CAMAC commands used.

Joerger ENTERPRISES, INC.

MODEL TR1012

10MHZ, 12 BIT TRANSIENT RECORDER

FEATURES:

- 10MHZ SAMPLING RATE
- 12 BIT RESOLUTION
- 256K MEMORY
- ACTIVE MEMORY PROGRAMMABLE
- INTERNAL OR EXTERNAL CLOCK
- CRYSTAL CONTROLLED INTERNAL CLOCK, PROGRAMMABLE
- SINGLE WIDTH CAMAC MODULE
- PRE/POST-TRIGGER OPERATION, PROGRAMMABLE

The MODEL TR1012 incorporates the latest developments in ADC's, memories and programmable logic to provide a 12 bit ADC that can operate at rates up to 10MHZ. Its speed, resolution and 256K memory makes it suitable for many applications. It operates in a pre/post-trigger mode which can be set programmably. To insure accurate performance it has a high impedance amplifier with a band width of 40MHZ followed by a sample and hold amplifier. All these features are packaged in a single width CAMAC module.

SPECIFICATIONS

ANALOG INPUT	±1.25v, 1.5M ohms input impedance, 50 ohms optional.
ANALOG INPUT (OPTIONAL)	±1.25v, 1K ohms input impedance, 50 ohms optional, full range offset.
OVERLOAD	20v D.C., 100v for 1msec.
BANDWIDTH	40MHZ
SAMPLING RATE	D.C. to 10MHZ
RESOLUTION	12 bits
LINEARITY	1LSB (Typ)
MEMORY	16K standard, 64K, 128K, 256K optional. Active memory is programmable.
PRE/POST-TRIGGER RATIO	0/8 "Post-Trigger Mode" to 7/8 programmable.
CLOCK	Internal or External clock.
EXTERNAL CLOCK	D.C. to 10MHZ, may be varied during data acquisition.
INTERNAL CLOCK	10MHZ crystal controlled clock, can be programmably set for 10MHZ, 5, 2, 1, 500KHZ, 200 or 100KHZ.
CLOCK OUT	A TTL clock is supplied which is the same frequency the module is programmed to operate.
START-STOP	A manual front panel switch is provided to manually operate the module.
ANALOG OUTPUT	An analog output with 12 bit resolution is provided to monitor the data that has been collected. It has a full scale output of ±1.5 volts and operates at 100KHZ.
SYNC	A TTL sync signal is provided to synchronize the analog output.
STOP	A TTL stop input is provided to terminate the cycle.

CAMAC COMMANDS

0o	Reads out module status which includes the programmably selected active memory, pre-trigger samples and the sampling frequency.
2o	Reads out the data in 2's compliment, sign extended to 16 bits. When the last active channel is read out a Q=0 response is generated. This signal must be preceded by an F17 which loads the first address.
3o	Reads module identity and the total amount of memory the module contains.
8o	Tests LAM, Q=1 if LAM is set and enabled.
9o	Activates a data acquisition cycle, clears LAM.
10o	Clears LAM.
16o	Sets modules status.

R1-R3 Pre-trigger	R5-R7 Sample Period	R9-R15 Active Memory
0 0/8 Active Mem.	0 100nsec.	0 2K
1 1/8 " "	1 200nsec.	1 4K
2 2/8 " "	2 500nsec.	2 6K
3 3/8 " "	3 1usec.	3 8K
4 4/8 " "	4 2usec.	'
5 5/8 " "	5 5usec.	'
6 6/8 " "	6 10usec.	'
7 7/8 " "	7 Ext. Clock	127 256K

17o	Enables readout mode, loads first address.
18o	Enables analog display if module not active.
24o	Disables LAM.
25o	Stop cycle trigger.
26o	Enables LAM.
27o	Tests LAM.
X	All commands generate an X response.
Q	F0 and F3 generate a Q response. If module is not active (taking data) commands F2, F16, F17 and F18 are operable and generate a Q response. A Q=1 is generated in response to F8 if LAM is set and enabled, and F27 if LAM is set.
L	An L response is generated if the cycle has been completed and the modules L response is enabled.
(Z+C)S2	Clears module.
POWER REQUIREMENTS	±6v, ±24v power backup for memory.
SIZE	Single width CAMAC module.
TEMPERATURE RANGE	20° to 50°C

JEI0589

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Joerger ENTERPRISES, INC.

PRODUCT SUMMARY

TRANSIENT RECORDERS

TR200	200MHZ, 8 BITS, 256K MEMORY, PROGRAMMABLE, (#2 CAMAC)
TR2/25	DUAL CHANNEL, 25MHZ, 8 BITS, 64K MEMORY PER CHANNEL, PROGRAMMABLE
TR1012	10MHZ, 12 BITS, 256K MEMORY, PROGRAMMABLE
TR	100KHZ, 12 BITS, 16K MEMORY, PROGRAMMABLE
VTR1	25MHZ, 8 BITS, 64K MEMORY, (VME)
ADC3216	32 CHANNELS, 16 BITS, 128K MEMORY, PROGRAMMABLE

ANALOG TO DIGITAL CONVERTERS

ADC3216	32 CHANNELS, 16 BITS, 128K MEMORY, PROGRAMMABLE
ADC-L	16 CHANNELS, 12 BITS, UPPER AND LOWER LIMITS ON EACH CHANNEL
ADC-64	64 CHANNELS, 12 BITS, 64 WORD MEMORY
ADC-32	32 CHANNELS, 12 BITS, 32 WORD MEMORY
ADC-16	16 CHANNELS, 12 BITS, 16 WORD MEMORY
ADC-P	16 CHANNELS, 12 BITS, 10uSEC CONVERSION SPEED, 16 WORD MEMORY
ADC-1616	16 CHANNELS, 16 BITS, INTEGRATING ADC, PROGRAMMABLE
ADC-1612	16 CHANNELS, 12 BITS, INTEGRATING ADC, PROGRAMMABLE
ISO-ADC	16 CHANNELS, 12 BITS, INDIVIDUALLY ISOLATED INPUTS

DIGITAL TO ANALOG CONVERTERS

DAC-16	16 CHANNELS, 12 BITS, REREADABLE INPUT REGISTERS
DAC-8	8 CHANNELS, 12 BITS, REREADABLE INPUT REGISTERS
D/A-16	2 CHANNELS, 16 BITS, REREADABLE INPUT REGISTERS
PSC	2 CHANNELS, 12 BITS, RELAY OUTPUTS FOR POWER SUPPLY CONTROL
XY	2 CHANNELS, 11 BITS PLUS SIGN, XY DRIVER

ANALOG MULTIPLEXERS

AM	15 CHANNELS, EXPANDABLE, RELAY SWITCHING
AMS	32 CHANNELS, EXPANDABLE, SOLID STATE SWITCHING, PROGRAMMABLE
ISO-AMP	16 CHANNELS, INDIVIDUALLY ISOLATED CHANNELS

STEPPING MOTOR CONTROLLERS AND DRIVERS

SMC-24	24 BITS, ACC./DEC., MANUAL MODE, REMOTE MODE,6 AMPS OPTICALLY ISOLATED
SMC-L	16 BITS, ACC./DEC., MANUAL MODE 6 AMPS OPTICALLY ISOLATED
SMC-R	DUAL CHANNEL, 16 BITS, MANUAL MODE, 2 AMPS OPTICALLY ISOLATED

POSITION ENCODERS

SDC	14 BIT SYNCHRO TO DIGITAL CONVERTER
IE	24 BIT INCREMENTAL ENCODER, PRESETTABLE, LIMIT DETECTION

SCALERS

S-12	12 CHANNEL, 24 BITS, 100MHZ
S-3	150MHZ, 12 BITS, DEADTIMELESS, 4K MEMORY, PROGRAMMABLE
S-2	10MHZ, 24 BITS, UP/DOWN PRESETTABLE COUNTER, GATE AND PULSE TRAIN OUT
S-1	4 CHANNELS, 200MHZ, 24 BITS, INDIVIDUAL INHIBITS
VS	DUAL CHANNEL, 200MHZ, 8 DIGIT READOUT, NIM
QVS	4 CHANNELS, 200MHZ, 8 DIGIT READOUT, 19" RACK

REGISTERS

QIR	4 CHANNELS, 24 BITS/CHANNEL, TTL
CS	24 BITS, OPTICALLY ISOLATED INPUTS, VISUAL DISPLAY
QOR	4 CHANNELS, 24 BITS/CHANNEL, TTL
OR	DUAL, 24 BITS, TTL, VISUAL DISPLAY
OR-1	DUAL, 24 BITS, 250MA DRIVE, VISUAL DISPLAY
OR-2	16 BITS, RELAY OUTPUTS, SELECTIVE SET/RESET, VISUAL DISPLAY
OR-3	16 BITS, OPTICALLY ISOLATED OUTPUTS, SELECTIVE SET/RESET, DISPLAY
OR-4	16 BITS, TTL, SELECTIVE SET/RESET, VISUAL DISPLAY
IR-1	DUAL 24 BIT INPUT, 24 BIT OUTPUT, TTL, VISUAL DISPLAY

MISCELLANEOUS

CCA-2	TYPE A2 CRATE CONTROLLER (#2 CAMAC)
VBT	VISUAL BRANCH HIGHWAY TERMINATOR (#2 CAMAC)
CG	10MHZ CLOCK GENERATOR, 8 DECADE OUTPUTS, ONE PROGRAMMABLE OUTPUT
DD	DATAWAY DISPLAY, 72 DATAWAY SIGNALS AND POWER LINES DISPLAYED
MI/O	MANUAL INPUT, VISUAL OUTPUT, 24 BITS, TEST UNIT

NOTE: All modules are packaged in single width CAMAC module unless otherwise specified.

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Jelge ENTERPRISES, INC.

DOMESTIC PRICE LIST

OCTOBER 1989

ADC3216-8	$2395
ADC3216-32	2795
ADC3216-64	3195
ADC-16	1295
ADC-32	1495
ADC-64	1795
ADC-L	1795
ADC-P	1395
ADC-1612	1195
ADC-1612P	1395
ADC-1616	1675
AM	995
AMS	1095
CCA-2	1595
CG	545
CG-100	595
CG-200	595
CS-5	695
CS-12	695
CS-24	695
CS-48	695
CS-120	745
CN/T	495
DAC-16	1295
DAC-8	895
DAC-8L	975
D/A-16	995
DD	495
FT-P	$ 495
GG	1295
IE	695
IR-1-D	795
ISO-ADC	2995
ISO-AMP	2095
MI/O	495
OR	595
OR-1	675
OR-2	595
OR-3	595
OR-4	545
PSC	1095
PSD (NIM)	645
QIR	845
QOR	845
SDC	1450
SMC-L	895
SMC-LP	1195
SMC-LHC	1195
SMC-LPHC	1475
SMC-24	995
SMC-24P	1295
SMC-24HC	1295
SMC-24PHC	1575
SMC-R	1125
SMC-R-REAR	1195
SMC-R-RELAY	1250
S1-1	$1195
S2	695
S3	1995
S-12	1495
TR	1850
TR-200-64	6595
TR-200-256	8995
TR2/25-8	2950
TR2/25-16	3150
TR2/25-32	3550
TR2/25-64	4350
TR1012-16	4495
VTR1 (VME)	3695
VBT	845
VBT-C	845
WT	595
XY	995
VS (NIM)	1095
QVS (RACK)	2795

F.O.B. NEW YORK USA

WARRANTY: ONE YEAR

TERMS: NET 30 DAYS

GSA PRICING AVAILABLE

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